REMARKS

I. STATUS OF CLAIMS

In accordance with 37 C.F.R. § 1.173(c), the status of the claims are as follows:

Claims 1-33 and 40-54 are pending in the reissue application.

Claims 1-33 are original claims and remain allowed. No changes have been made to claims 1-33.

Claims 34-54 were previously added in the preliminary amendment filed November 24, 2003, with claims 34-39 being canceled in the enclosed amendment.

Claims 40 and 47 are being amended in the enclosed amendment.

No new matter has been added.

II. EXPLANATION OF SUPPORT IN DISCLOSURE FOR AMENDMENTS

Claims 40 and 47 have been amended to include the following recitations: "wherein the maximum bit length of an instruction that is executed in parallel is M bit, M being an integer" and "an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the bit width of the instruction bus is shorter than M * N bits."

Support for the aforementioned features of the present invention can be found, for example, in Figures 4, 7 and 11 of Applicants' drawings and the corresponding disclosure in Applicants' specification. For example, one exemplary embodiment is shown in Figure 4 (illustrating relationship between instruction register 23 which is a part of the instruction supplying/issuing unit 20 and decoding unit 30) with corresponding disclosure at col. 9, lines 11-15 of parent USP No. 6,324,639. Specifically, the specification discloses that the "the instruction register 23 is composed of four 21-bit registers and stores the four units that are transferred from

the instruction buffer 22 [whereby the] instruction register 23 issues up to four of these units to the decoding unit 30." Accordingly, as configured in this exemplary embodiment, the bus width would be 84 bits which is shorter than M * N (noting that M is 42 bits for the maximum two-unit instruction while N is 3 for the three decoders 33-35).

III. PRIOR ART REJECTION

Claims 34-54 stand rejected under 35 U.S.C. § 102 as being anticipated by Eickemeyer et al. '746 ("Eickemeyer"). Claims 36-39 have been canceled without prejudice/disclaimer to the subject matter embodied thereby, rendering the rejection against them moot. Claims 40 and 47 are the remaining rejected independent claims. This rejection is respectfully traversed for the following reasons.

Claims 40 and 47 each embody an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the bit width of the instruction bus is shorter than M * N bits; where M is the maximum bit length of an instruction that can be executed in parallel and N is the number of instructions that can be executed in parallel. In direct contrast, Eickemeyer expressly discloses (col. 12, lines 5-14):

> the rule for compounding a set of instructions which includes variable instruction lengths provides that all instructions which are 2 bytes or 4 bytes long are compoundable with each other. That is, ... a 4 byte instruction is capable of parallel execution with another 2 byte ***or another 4 byte instruction***. The rule further provides that all instructions which are 6 bytes long are not compoundable. (emphasis added)

Accordingly, Eickemeyer discloses only a conventional bus configuration having a bus width which is sufficient to handle processing the maximum bit size. For example, if the system is designed to enable execution of 3 instructions in parallel (N=3) each having a maximum size of 42 bits (M=42), then the bus width would be ***equal*** to (N * M = 3 * 42) to allow three-42 bit

instructions to be processed, whereas in the present invention the bus width is shorter than N * M.

Turning back to Eickemeyer, the disclosed maximum bit length of an instruction that is executed in parallel is 4 bits so that M = 4, noting that Eickemeyer expressly states in the cited portion above "that all instructions which are 6 bytes long are not compoundable" (though Eickemeyer references "bytes," because the analysis does not change, they are being equated to "bits" throughout this discussion for simplicity). Further, the number of instructions which are executed in parallel is 2 so that N = 2. Accordingly in Eickemeyer, M * N = 4 * 2 = 8, and Eickemeyer further discloses that a 4 "bit" instruction is capable of parallel execution with ***another 4 byte instruction*** so that the bus width must be at least 8 bits to accommodate two 4 "bit" instructions. The result will be the same for any value of M and N as Eickemeyer discloses a conventional bus configuration designed to accommodate parallel processing for the maximum number and length of instructions. That is, like conventional systems, the bus width of Eickemeyer is at least ***equal*** to M * N, so as to accommodate parallel processing where each of the instructions to be executed in parallel can be the maximum bit size.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Eickemeyer does not anticipate claims 40 and 47, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are

contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 40 and 47 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

IV. CONCLUSION

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
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